

Semiconductor

Competition heating up among foundries

Samsung Electronics and GlobalFoundries to increase capex

Samsung Electronics (SEC) and GlobalFoundries (GF) are planning to take aggressive approaches to capex going forward. SEC, the world's fourth-largest foundry player, has initiated 10nm production ahead of global leader TSMC, and plans to install next-generation extreme ultraviolet (EUV) lithography equipment before its rivals do. The company has also started construction on its first new system LSI fab in years. Meanwhile, GF, the world's second-largest player, is pushing forward with the adoption of the 22nm fully-depleted silicon-on-insulator (FD-SOI) process. Additional capex plans include the expansion of existing fabs and construction of a new fab in Chengdu, China.

TSMC also plans to increase capex

Unsurprisingly, global leader TSMC is not content to stand pat while rivals ramp up capex. At a recent investor event, the company announced its new technology road map, which includes the adoption of new processes such as 22nm ultra-low power (ULP), 12nm FinFET compact (FFC), and 7+nm EUV lithography. TSMC's plan to adopt EUV lithography for the 7+nm process is particularly noteworthy, as the company has been more conservative than its rivals with regard to the technology. Indeed, TSMC had initially planned to start using EUV technology upon migration to 5nm, but SEC's aggressive stance appears to have compelled the company to move more quickly. Meanwhile, 22nm ULP and 12nm FFC were newly developed in response to GF's 22nm FD-SOI and SEC's 10nm process technologies.

Foundry capex to grow

Stiffening competition among foundries should affect the semiconductor industry in the following ways:

- 1) EUV lithography equipment is likely to be used for 7+nm processes (starting in 2018), led by SEC and TSMC; previously, foundries had planned to start adopting the technology at 5nm. As such, EUV-related companies, such as equipment maker ASML and vacuum pump producer LOT Vacuum, will be key beneficiaries. On the other hand, companies exposed to existing deposition and etching processes may be negatively affected.
- 2) Adoption of FD-SOI should begin in earnest. After losing ground to FinFET, FD-SOI, which was initially developed by STMicroelectronics, has re-entered the spotlight, thanks to GF's and SEC's plans to adopt the technology. FD-SOI offers notable advantages with regard to the production of low-power chips for IoT applications. France-based Soitec stands to benefit the most from FD-SOI adoption, as it is the exclusive supplier of FD-SOI substrates.
- 3) Investment in semiconductor equipment should grow visibly, with SEC, GF, and TSMC all planning to build new fabs to increase total capacity. The adoption of EUV and FD-SOI technologies will require significant production process changes, which will stimulate spending on new equipment and materials. It should be noted that, among domestic players, Wonik IPS supplies deposition equipment to foundries.

I. Competition heating up among foundries

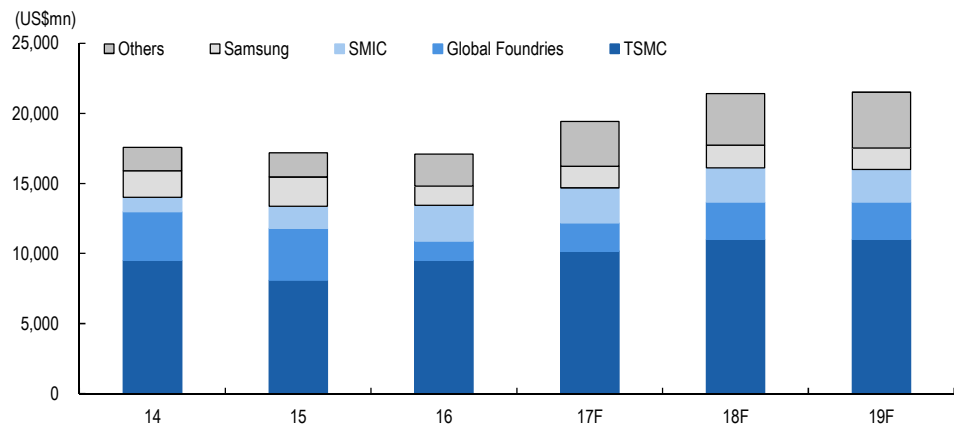
Taiwan-based TSMC, the global leader among semiconductor foundries, recently unveiled its technology road map at an investor event. The company controls more than half of the global market, and is the final producer of numerous key semiconductors used in smartphones and PCs. As such, the announcement was closely watched by industry experts and investors.

Notably, TSMC plans to adopt 22nm ULP, 12nm FFC, and 7+nm EUV. All three processes are new to TSMC's technology road map and outside of current industry standards. The radical changes to the technology road map clearly show that TSMC intends to widen the gap with latecomers, such as SEC and GF.

SEC and GF, on the other hand, are aggressively pursuing the adoption of new processes, in order to gain on TSMC. Notably, both companies are increasingly threatening TSMC, as they are ramping up investments in new fabs. Going forward, we expect stiffening competition among foundries to affect the semiconductor industry in the following ways:

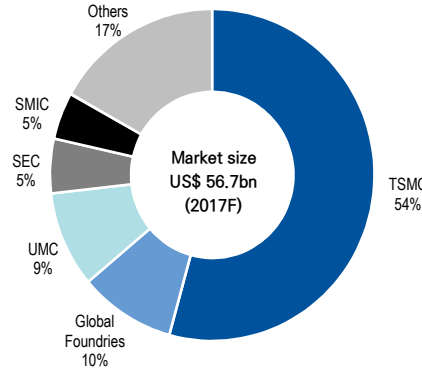
- 1) Adoption of EUV should accelerate.
- 2) Orders for semiconductor equipment should visibly grow amid increased foundry capex.
- 3) Adoption of the FD-SOI process should begin in earnest.
- 4) Markets for IoT-use and low-power semiconductors should meaningfully expand.

Figure 1. Global foundry CAPEX trend



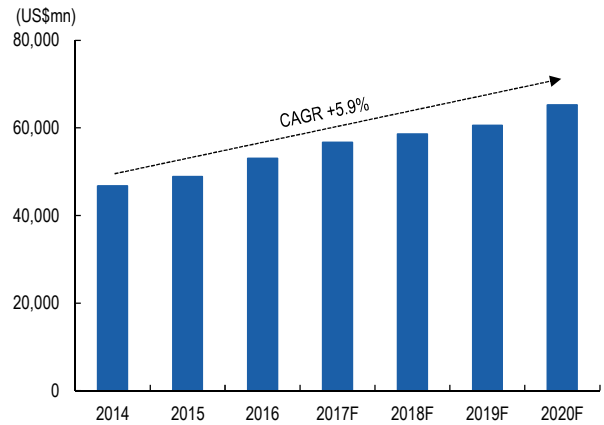
Source: Gartner, Mirae Asset Daewoo Research

Figure 2. Global foundry market share



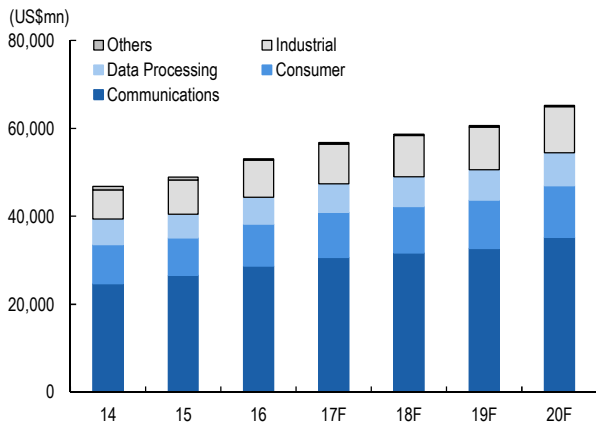
Source: Gartner, Mirae Asset Daewoo Research

Figure 3. Global foundry market trend and forecast



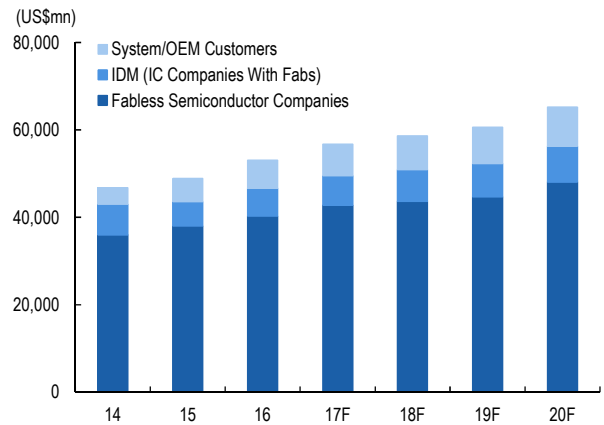
Source: Gartner, Mirae Asset Daewoo Research

Figure 4. Global foundry market trend by application



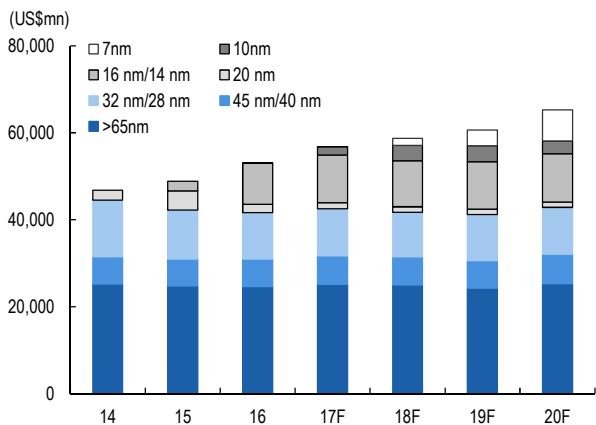
Source: Gartner, Mirae Asset Daewoo Research

Figure 5. Global foundry market trend by customer type



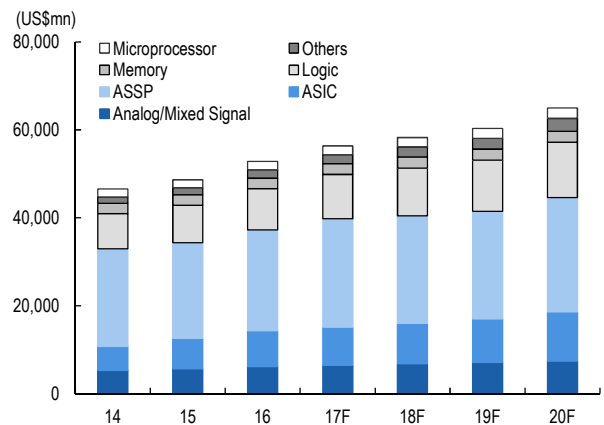
Source: Gartner, Mirae Asset Daewoo Research

Figure 6. Global foundry market trend by line width



Source: Gartner, Mirae Asset Daewoo Research

Figure 7. Global foundry market trend by device



Source: Gartner, Mirae Asset Daewoo Research

Table1. Global foundry companies' earnings table (Wbn)

	Market Cap.	Revenue			OP			Net profit		
		16	17F	18F	16	17F	18F	16	17F	18F
SEC	295,708	201,867	223,041	226,703	29,241	37,969	37,589	22,412	29,013	29,273
TSMC	182,443	34,126	37,960	41,432	13,605	15,211	16,565	12,033	13,374	14,569
UMC	5,760	5,323	5,750	5,989	232	188	292	299	291	342
SMIC	7,218	2,532	3,319	3,980	251	422	448	287	429	440

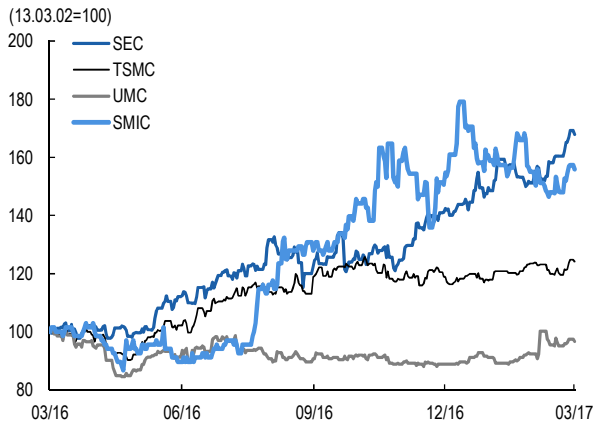
Source: Bloomberg, Mirae Asset Daewoo Research

Table2.. Global foundry companies' valuation table (% , x)

	ROE			PER			PBR		
	16	17F	18F	16	17F	18F	16	17F	18F
SEC	12.7	15.1	13.5	13.2	10.7	10.6	1.5	1.4	1.3
TSMC	25.6	24.2	23.7	14.8	13.7	12.5	3.6	3.1	2.8
UMC	3.8	3.6	4.1	18.2	19.1	16.8	0.7	0.7	0.7
SMIC	9.6	9.4	9.1	33.9	16.4	15.5	1.4	1.4	1.3
Average	12.9	13.1	12.6	20.0	15.0	13.9	1.8	1.7	1.5

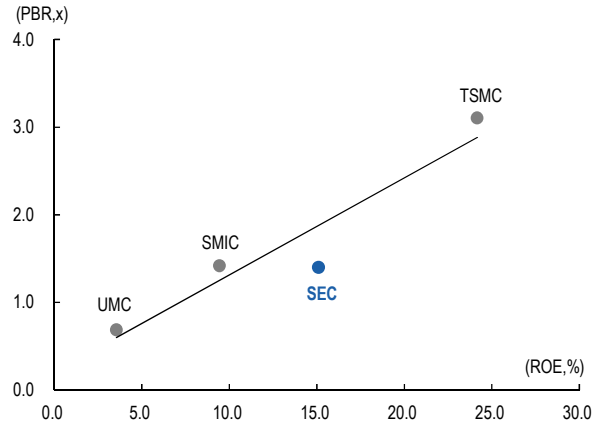
Source: Bloomberg, Mirae Asset Daewoo Research

Figure 8. Foundry companies' relative share price trend



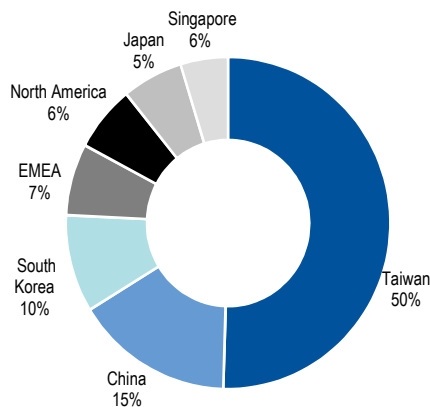
Source: Bloomberg, Mirae Asset Daewoo Research

Figure 9. Foundry companies' PB-ROE chart



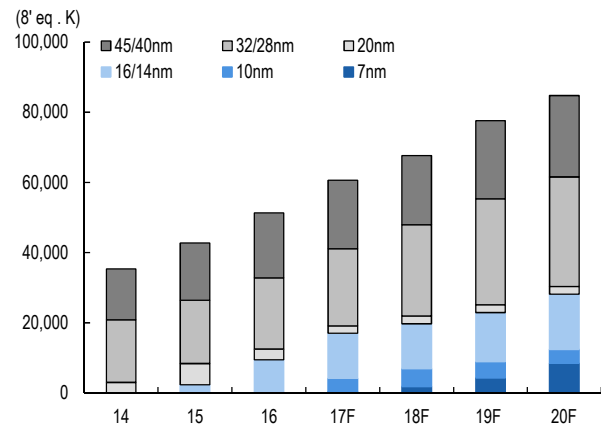
Source: Bloomberg, Mirae Asset Daewoo Research

Figure 10. Capacity ratio by region



Source: Gartner, Mirae Asset Daewoo Research

Figure 11. Capacity trend by line width



Source: Gartner, Mirae Asset Daewoo Research

II. Growing focus on EUV and FD-SOI

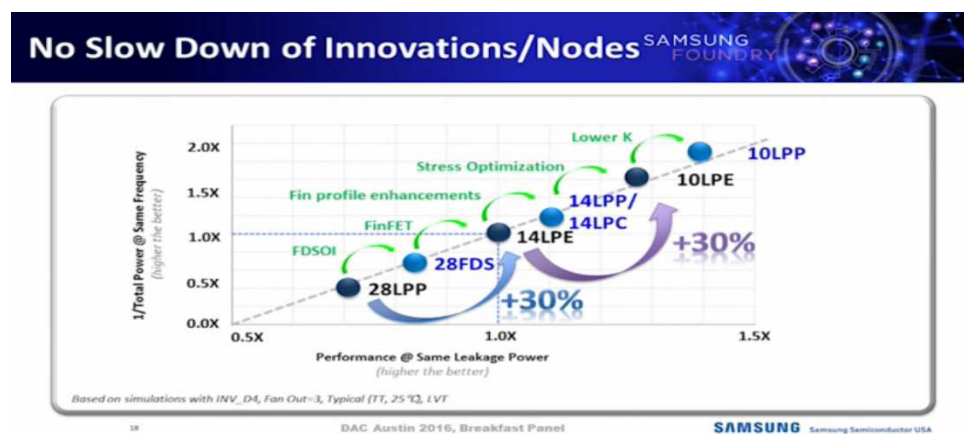
1. SEC and GF to aggressively increase capex

SEC and GF are planning to aggressively expand system LSI capex, in a bid to gain on the current global leader, TSMC. Previously, SEC had reduced its focus on system LSI investments, after its 14nm FinFET process technology failed to displace TSMC's 16nm FinFET. In addition, the loss of major clients, such as Apple to TSMC, weighed on SEC's system LSI investment outlook. Although market watchers had expected SEC to acquire new customers, potential clients, including NVIDIA, continued to prefer TSMC. Meanwhile, GF, the second-largest foundry in the world, has found itself stuck in a similar situation. Failing to develop 14nm FinFET technology on its own, GF entered into a technological partnership with SEC, losing some clients to TSMC in the process. Against this backdrop, SEC and GF saw their market shares stagnate, while TSMC continued to enjoy peak earnings over several years.

Recently, however, SEC and GF have started to take aggressive approaches to capex. At end-2016, SEC initiated 10nm FinFET production of Snapdragon 835 and Exynos processors for Galaxy S8 smartphones. Meanwhile, TSMC has yet to initiate production on 10nm FinFET. Now, SEC is planning to resume spending on production equipment to expand its capacity for the first time in years. We expect the company to build a new production line next to its existing fab in Hwaseong, Korea.

In addition, SEC's plans for the adoption of next-generation EUV lithography equipment are far more ambitious than those of its peers. Indeed, while TSMC and Intel had initially planned to adopt EUV lithography equipment starting with 5nm processes (2019), SEC announced that it would use EUV equipment for 7nm (early 2018). The Korean electronics giant's decision to speed up adoption has sent shockwaves through the industry, prompting rivals to reconsider their plans. We note that GF is also displaying newfound aggressiveness, with the company currently focusing on the adoption of FD-SOI, while also making plans for the development of a proprietary 7nm process technology. Additional capex plans announced by GF include the expansion of its existing fabs and construction of a new fab in Chengdu, China.

Figure 12. SEC's node change trend



Source: SEC

Figure 13. SEC's System LSI fab



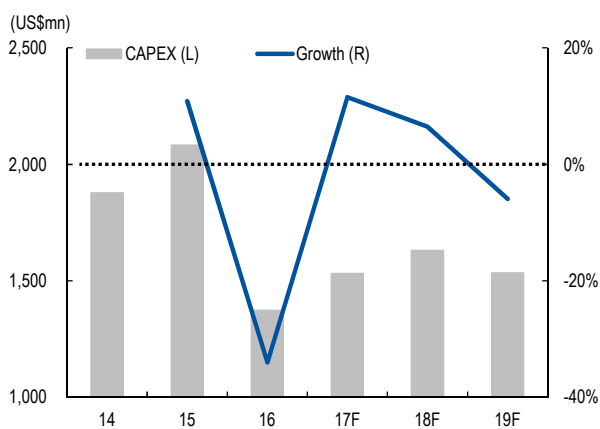
Source: Google

Figure 14. Global Foundries' fab



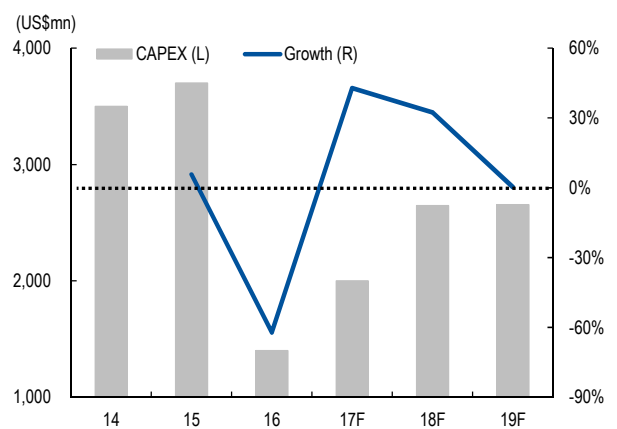
Source: Global Foundries

Figure 15. SEC foundry CAPEX trend



Source: Mirae Asset Daewoo Research

Figure 16. Global Foundries' CAPEX trend



Source: Gartner, Mirae Asset Daewoo Research

2. TSMC also plans to increase capex

Unsurprisingly, TSMC is not content to stand pat while SEC and GF ramp up capex. The company recently unveiled its new technology road map, which focuses on the adoption of three new process technologies. The company's plans to accelerate EUV lithography adoption are particularly noteworthy, as TSMC has been more conservative than its rivals, regarding the adoption of next-generation lithography equipment. TSMC had initially planned to start using EUV lithography equipment following migration to 5nm, but decided to pull forward the timing by one generation (7+nm), in light of SEC's aggressive stance. Indeed, the Korean giant recently announced plans to use EUV for the 7nm process (2018), and has been actively placing orders for EUV lithography and production equipment.

We believe that SEC, a latecomer to the foundry industry, is seeking to disrupt the market via the early adoption of EUV lithography equipment. Although the economic viability of EUV lithography equipment has yet to be confirmed, SEC is pursuing 7nm adoption, in a bid to jump ahead of the market leader. In contrast, market leader TSMC had originally planned to start adopting EUV lithography equipment from 5nm to minimize risk.

The productivity of EUV equipment has been rapidly improving, with ASML recently announcing that its EUV equipment was capable of exposing over 1,600 wafers per day. Once it is capable of handling 2,000 wafers per day, EUV equipment will surpass conventional argon fluoride immersion (ArF-i) equipment, in terms of productivity. Just one year ago, EUV lithography equipment was only capable of exposing around 1,250 wafers per day.

Against this backdrop, it now appears that TSMC believes the potential positives from early adoption of EUV equipment outweigh the risks, paving the way for the company to pursue 7+nm EUV adoption. The 7+nm process is an upgraded version of 7nm, offering 10% faster speeds while consuming 15% less power. The early adoption of EUV lithography equipment should benefit companies in the EUV equipment supply chain. As EUV lithography equipment requires a whole new array of parts and materials (including laser sources, transmissive masks, vacuum chambers, reflective masks, photoresists, and pellicles), its adoption should usher in significant changes to the semiconductor equipment industry.

Companies capable of quickly developing relevant parts and materials should benefit in the near term. At present, key beneficiaries include EUV equipment maker ASML and domestic vacuum pump producer LOT Vacuum. Meanwhile, after benefiting from the slower-than-expected resolution enhancement of conventional lithography equipment, companies supplying equipment and materials for deposition and etching processes should now be negatively affected by the adoption of EUV equipment. TSMC demonstrated that the adoption of EUV equipment will reduce the number of patterning steps (deposition and etching steps) from four (quadruple patterning) to one (single patterning). Companies supplying conventional deposition and etching equipment will need to diversify their product portfolios by developing items likely to benefit from the adoption of EUV equipment, such as vacuum, ALD, and micro-deposition equipment.

Figure 17. Resolution and depth of focus equation

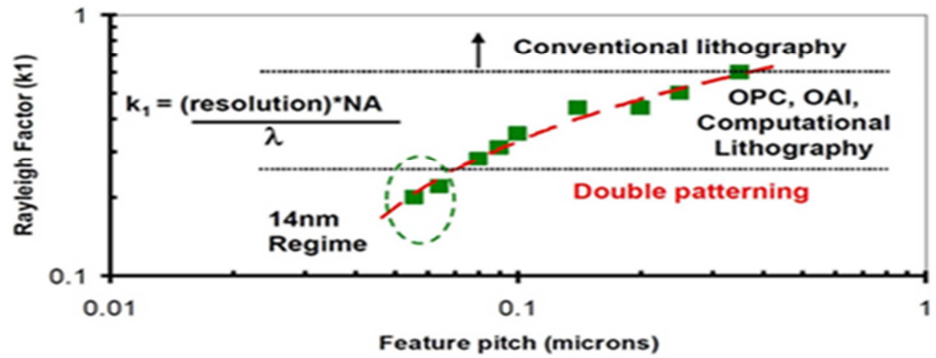
$$R = k_1 * \frac{\lambda}{NA} = k_1 \frac{\lambda}{n \sin \theta} = k_1 \frac{\lambda/n}{\sin \theta}$$

$$DOF = K_2 \frac{\lambda}{n \sin^2 \theta} = k_2 \frac{\lambda/n}{\sin^2 \theta} = k_2 \frac{n\lambda}{NA^2}$$

R=Resolution, DOF=Depth of Focus, NA=Numerical Aperture, n=Refractive Index, λ=Exposure Wavelength, k1, k2=Process Factor

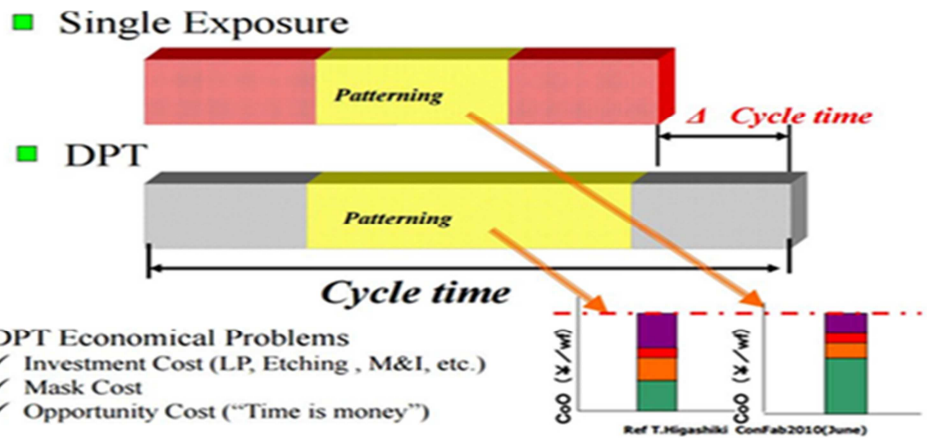
Source: Mirae Asset Daewoo Research

Figure 18. With limitations of lithography equipment, double patterning is key technology



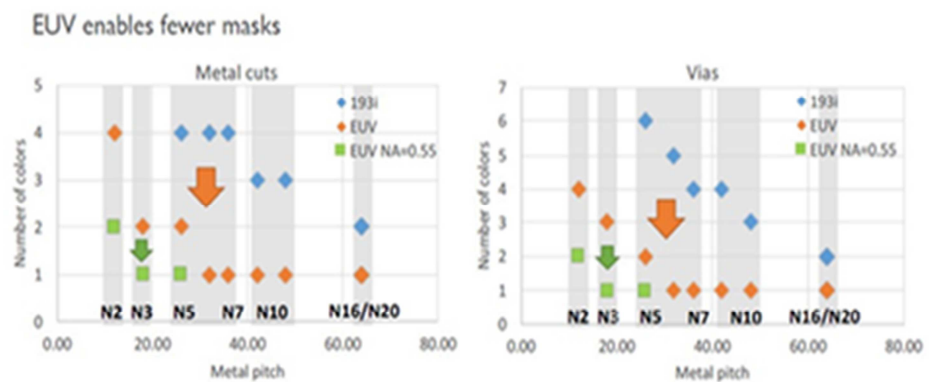
Source: IBM

Figure 19. Double patterning economic problems



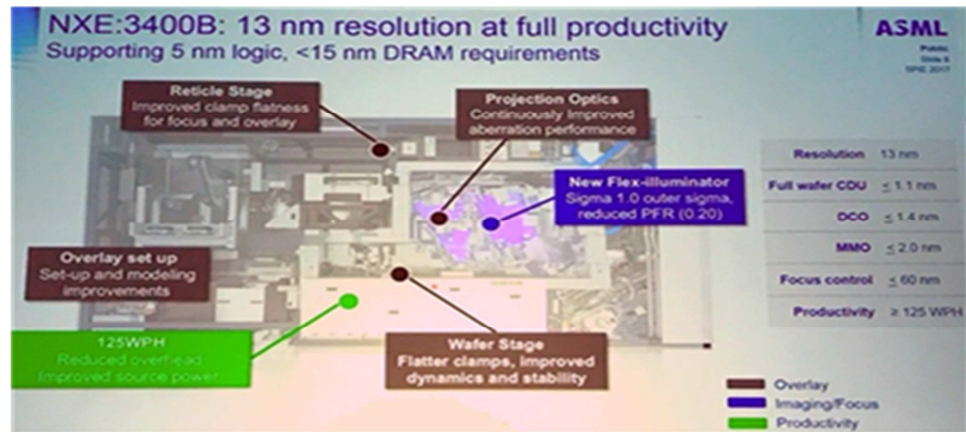
Source: Toshiba

Figure 20. EUV enabling fewer masks



Source: ASML

Figure 21. ASML's latest EUV model



Source: ASML

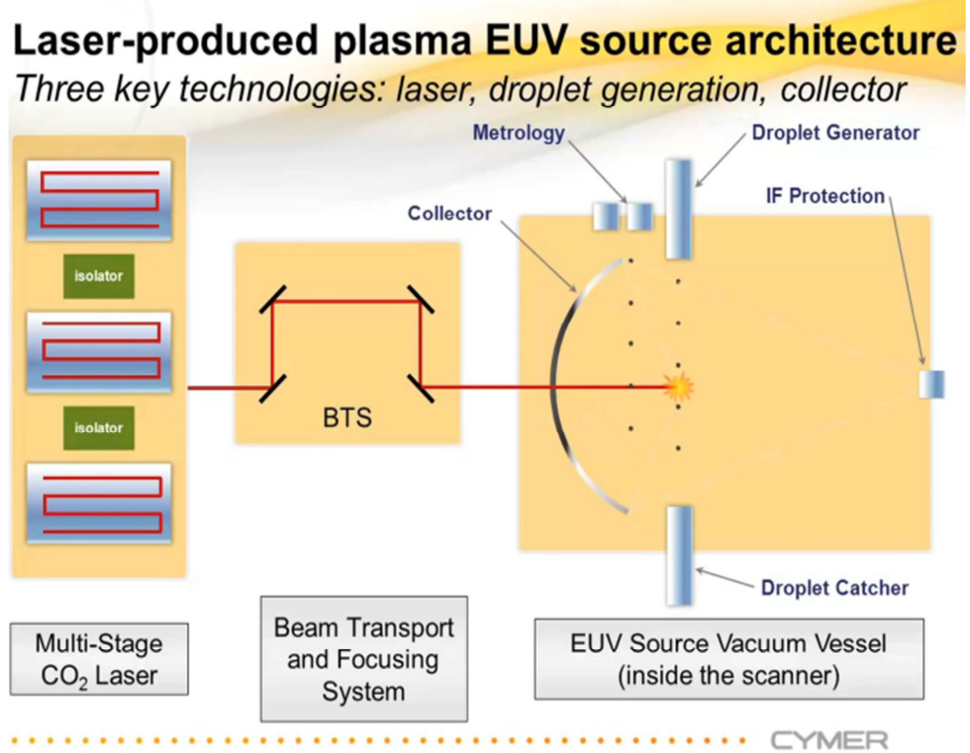
Figure 22. Number of masks (ArF-I, 20nm vs. ArF-I, 10nm and ArF-I 7 nm vs. ArF-I+ EUV 7nm)

Layer	ArF-I, 20nm	Number of Masks	ArF-I, 10nm	Number of Masks
Fin	ArF-I SP	1	SADP+SP Cut	2
Gate	ArF-I+SP Cut	2	SADP+SP Cut	2
MOG	ArF-I+Block	2	LELE	2
MOA	ArF-I+Block	2	LELELE	3
V0	LELE	2	LELE	2
M1	LELE	2	LELELE	3
V1	ArF-I SP	1	LELE	2
M2	ArF-I SP	1	SADP+Block	2
Total		13		18

Layer	ArF-I, 7nm	Number of Masks	ArF-I+ EUV, 7nm	Number of Masks
Fin	SAQP+LELE Cut	3	ArF-I SAQP+EUV SE EUV	2
Gate	SADP+SP Cut	2	ArF-I SADP+SP Cut	2
MOG	LELE	2	ArF-I LELE	2
MOA	SADP+LELELELE Block	6	ArF-I SADP+EUV SE Block	2
V0	LELELE	3	EUV SE	1
M1	SAQP+LELELE Block	4	ArF-I SADP+EUV SE Block	2
V1	LELELE	3	EUV SE	1
M2	SAQP+LELELE Block	4	ArF-I SAQP+EUV Block	2
Total		27		14

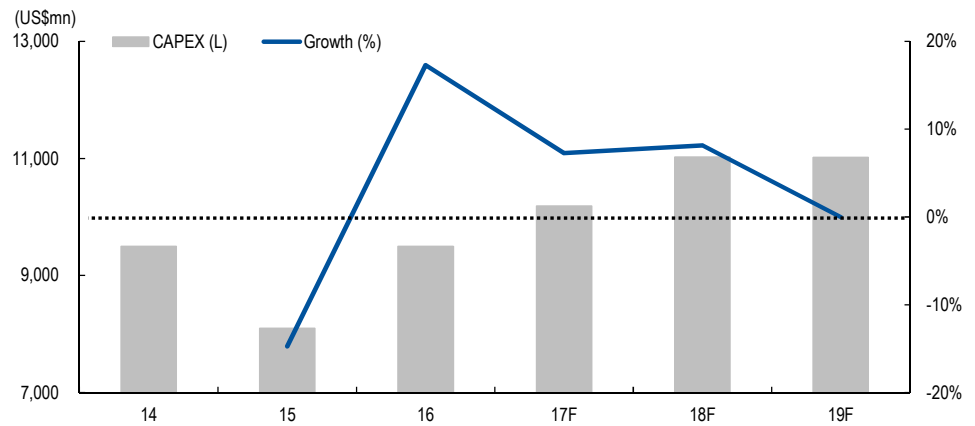
Source: Mirae Asset Daewoo Research

Figure 23. Laser-produced plasma EUV source architecture



Source: SPIE

Figure 24. TSMC CAPEX trend



Source: Gartner, Mirae Asset Daewoo Research

3. Intensifying competition among foundries to drive up equipment investments

We expect fierce competition between major players, such as TSMC, SEC, and Global Foundries (GF), to lead to greater semiconductor investments. We estimate that total investments by foundries will increase from US\$17.2bn in 2015 to US\$21.4bn in 2018. TSMC recently announced the extension of its technology roadmap to include 12nm and 22nm processes to counter the aggressive moves of their rivals. Currently, the industry norms stand at 14/16nm, 20nm and 28nm. GF began to mass-produce 22nm FD-SOI, and SEC is expanding their 28nm FD-SOI process. We expect TSMC's 22nm process to compete against SEC and GF's FD-SOI.

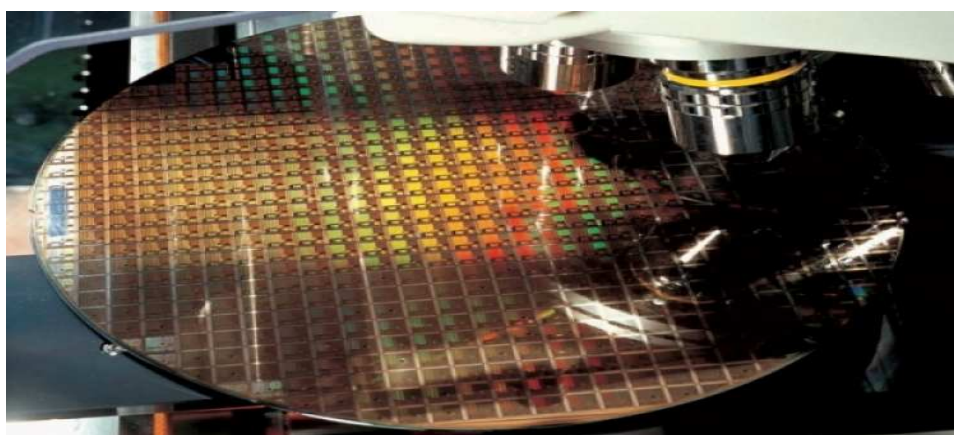
FD-SOI is a process technology that adds a very thin oxide insulator layer beneath the silicon transistor, greatly reducing leakage currents to the silicon wafer substrate versus traditional bulk CMOS.

FD-SOI offers an alternative to the mainstream FinFET technology. The FD-SOI process was developed by ST Microelectronics, with Soitec (France) producing SOI wafers. While the adoption of the FinFET process technology by leading players, such as Intel and SEC, raised uncertainties over the deployment of FD-SOI technology in mass production, the recent adoption of FD-SOI technology by GF and SEC is renewing market interest. FD-SOI requires fewer processing steps and incurs lower cost, compared with FinFET. Bulk CMOS requires deep implants to reduce current leakage, whereas FD-SOI only contains the buried oxide layers and requires no doping in the channel, making it fully depleted. GF's 22nm FD-SOI process, called 22FDX 22nm, uses 10% fewer masks than bulk CMOS' 28nm process.

Through a new 22nm process, we think TSMC is seeking to keep rivals in check, given the likely proliferation of FD-SOI applications. As IoT-enabled devices, especially RF chips, need power-efficient chips, rather than high-performance chips, FD-SOI is a more appealing option than FinFET. As such, the market is expected to be split between FinFET for high-performance chips, such as application processors (AP) and FD-SOI for IoT applications.

We think TSMC's 22nm process is a move to fend off the FD-SOI process, which has strong potential in the IoT market. TSMC seeks to prevent a large-scale shift of chips using the existing 28nm process toward 22nm FD-SOI chips. TSMC says that FD-SOI process offered by rivals requires customers to redesign chips and do not have the comprehensive IP ecosystem. In contrast, TSMC underlines that its 22nm will allow customers to use their existing design. TSMC claims that its 22nm node uses the same mask counts, design rules, and SRAM bit cells as its 28HPC+ node.

Figure 25. TSMC's 12nm wafer



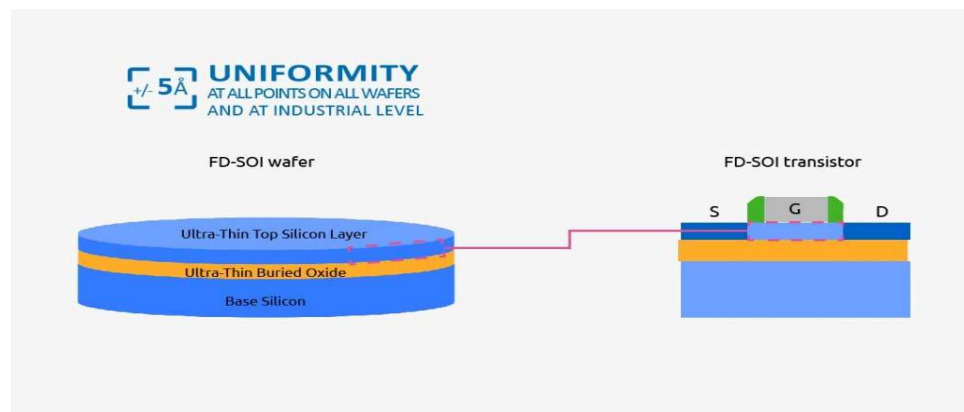
Source: TSMC

The FD-SOI camp is also upping its ante. GF and ST Microelectronics are planning to further expand their FD-SOI capacity from the current 10,000 wafers per month. Sony is looking to use FD-SOI for the image signal processor (ISP) on stacked CMOS Image Sensors (CIS). NXP Semiconductors recently announced its plan to introduce FD-SOI technology to its processors.

TSMC's 12nm process presents a counterweight to SEC's 10nm process. As aforementioned, SEC outpaced TSMC in its transition to the 10nm process. Initially, TSMC skipped 10nm in the face of yield issues to focus on 7nm. However, in response to growing importance of the 10nm process, TSMC introduced an upgraded version of the existing 16nm process to prevent its customers from defecting to SEC's 10nm process.

We expect growing competitive pressure to stimulate semiconductor investments. GF announced that it would build a 300mm wafer fab for 22nm FD-SOI in Chengdu China and plans to expand its 14nm FinFET capacity at its Fab 8 facility in New York by an additional 20%, and 40nm capacity at its 300mm fab in Singapore by 35%. SEC has not expanded its foundry capacity for years, but has begun to build new fabs. TSMC plans to expand its investments to meet the competition. As FD-SOI brings about changes to conventional semiconductor processes, it requires new investments and will likely benefit Wonik IPS, a system LSI-use deposition equipment manufacturer, among Korean equipment vendors, and Soitec, a FD-SOI wafer manufacturer, among overseas vendors.

Figure 26. FD-SOI process



Source: STMicro

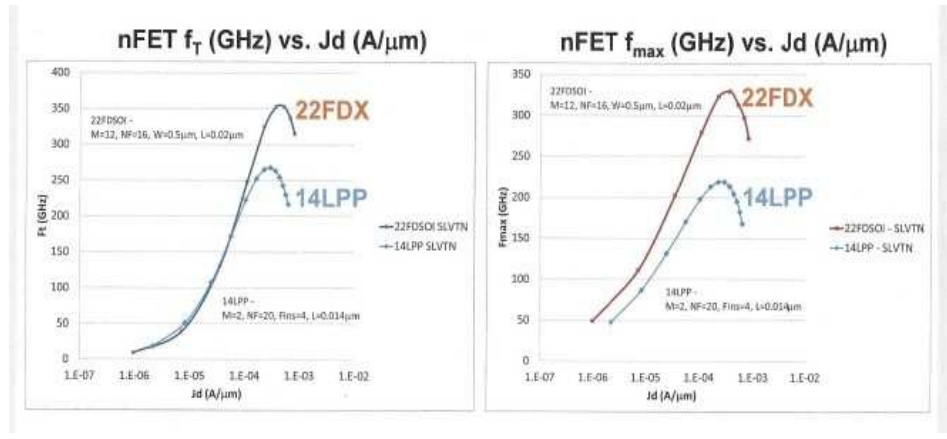
Figure 27. FinFET vs. FD-SOI (structure)

Fully-Depleted Advanced Technology Architectures

FINFET	FDSOI
<ul style="list-style-type: none"> - Best electrostatics (DIBL, SS) - Highest Drive Current (per unit area) - Higher Ceff (including high Miller component from region between FINS) - Sources of variability (Dfin, Hfin, Fin taper) - Undoped/low fin doping → good RDF - Quantized active width – but better active efficiency in standard cells (improved PPA) - Higher process complexity 	<ul style="list-style-type: none"> - Good electrostatics (DIBL, SS) - Lower drive current due to simpler process - Lower Ceff - Sources of variability (Tsi, Tbox) - Undoped channel device → better RDF and device matching - Lower process complexity offsets higher substrate cost - Back Bias management is critical (back gate doping, power routing)
<p>Most suited for high performance applications</p>	<p>Most suited for low power / low leakage applications</p>

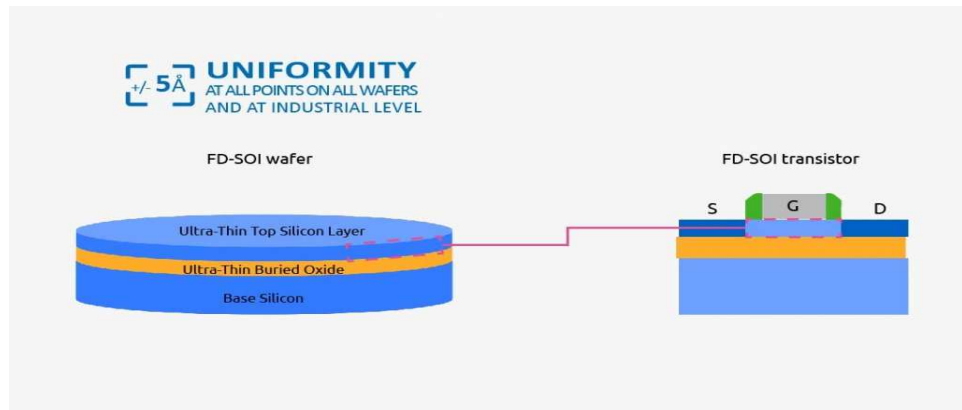
Source: Global Foundries

Figure 28. FinFET vs. FD-SOI (performance)



Source: Global Foundries

Figure 29. FD-SOI structure



Source: Soitec

Figure 30. FD-SOI related companies

FD-SOI Fast Growing Ecosystem 24

Ecosystem

- Products
- Services
- IPs
- Tools & EDA
- Wafer & Foundry

Source: Soitec

APPENDIX 1

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